

**What is claimed is:**

1. A line scan sensor comprising:  
first and second rows of pixels;  
corresponding first and second readout registers;  
a plurality of first channel structures, each channel structure of the first channel structures being disposed between a corresponding pixel of the first row of pixels and a corresponding register element of the first readout register; and  
a plurality of second channel structures, each channel structure of the second channel structures being disposed between a corresponding pixel of the second row of pixels and a corresponding register element of the second readout register.
2. The sensor of claim 1, further comprising:  
a first clocking structure disposed over and transverse to the plurality of first channel structures, wherein the first clocking structure includes a transfer gate electrode and a delay well electrode; and  
a second clocking structure disposed over and transverse to the plurality of second channel structures, wherein the second clocking structure includes a transfer gate electrode and a delay well electrode.
3. The sensor of claim 2, wherein:  
the first clocking structure further includes a storage well electrode disposed so that the delay well electrode is located between the storage well electrode and the transfer gate electrode of the first clocking structure; and  
the second clocking structure further includes a storage well electrode disposed so that the delay well electrode is located between the storage well electrode and the transfer gate electrode of the second clocking structure.
4. The sensor of claim 1, wherein each pixel of each row of pixels includes one of a photo diode and a pinned photo diode.

5. A method of using the sensor of claim 2 comprising steps of:  
applying a transfer clock pulse to the transfer gate electrode of the first clocking structure and the transfer gate electrode of the second clocking structure;  
applying a first delay clock pulse to the delay well electrode of the first clocking structure after the transfer clock pulse is applied; and  
applying a second delay clock pulse to the delay well electrode of the second clocking structure before the transfer clock pulse is applied.
6. A line scan sensor comprising:  
first and second rows of pixels;  
corresponding first and second readout registers;  
a first clocking structure disposed between the first row of pixels and the first readout register, wherein the first clocking structure includes a transfer gate electrode and a delay well electrode.
7. The sensor of claim 6, wherein the first clocking structure further includes a storage well electrode disposed so that the delay well electrode is located between the storage well electrode and the transfer gate electrode of the first clocking structure.
8. The sensor of claim 6, further comprising a second clocking structure disposed between the second row of pixels and the second readout register wherein the second clocking structure includes a transfer gate electrode and a delay well electrode.
9. The sensor of claim 8, wherein the second clocking structure further includes a storage well electrode disposed so that the delay well electrode is located between the storage well electrode and the transfer gate electrode of the second clocking structure.
10. The sensor of claim 8, further comprising:  
a plurality of first channel structures coupled between the first row of pixels and the first readout register, each channel structure of the first channel structures being disposed

under and transverse to the first clocking structure and between a corresponding pixel of the first row of pixels and a corresponding register element of the first readout register; and a plurality of second channel structures coupled between the second row of pixels and the second readout register, each channel structure of the second channel structures being disposed under and transverse to the second clocking structure and between a corresponding pixel of the second row of pixels and a corresponding register element of the second readout register.

11. A method of using the sensor of claim 8 comprising steps of:  
applying a transfer clock pulse to the transfer gate electrode of the first clocking structure and the transfer gate electrode of the second clocking structure;  
applying a first delay clock pulse to the delay well electrode of the first clocking structure after the transfer clock pulse is applied; and  
applying a second delay clock pulse to the delay well electrode of the second clocking structure before the transfer clock pulse is applied.
12. A method of using the sensor of claim 6 comprising steps of:  
applying a transfer clock pulse to the transfer gate electrode of the first clocking structure; and  
applying a first delay clock pulse to the delay well electrode of the first clocking structure after the transfer clock pulse is applied.
13. The sensor of claim 6, wherein each pixel of each row of pixels includes one of a photo diode and a pinned photo diode.
14. A line scan sensor comprising:  
first and second rows of pixels;  
a delay register coupled to the first row of pixels;  
a first readout register coupled to the delay register; and  
a second readout register coupled to the second row of pixels.

15. The sensor of claim 14, further comprising a summation circuit to combine serial outputs from the first and second readout registers.

16. The sensor of claim 14, wherein each pixel of the first and second row of pixels includes one of a photo diode and a pinned photo diode.

17. The sensor of claim 14, wherein each pixel of the first and second row of pixels includes a storage well and one of a photo diode and a pinned photo diode.

18. A method comprising steps of:  
 applying a transfer clock pulse to a transfer gate electrode of a first clocking structure and a transfer gate electrode of a second clocking structure;  
 applying a first delay clock pulse to a delay well electrode of the first clocking structure after the transfer clock pulse is applied; and  
 applying a second delay clock pulse to a delay well electrode of the second clocking structure before the transfer clock pulse is applied.

19. A method comprising a first step followed by a second step, wherein the first step includes steps of:  
 transferring photo charges in a delay register into a first readout register;  
 transferring photo charges in a first storage register into the delay register; and  
 transferring photo charges in a second storage register into the second readout register, and wherein the second step includes steps of:  
 collecting photo charges in the first storage register;  
 collecting photo charges in the second storage register;  
 shifting photo charges in a first readout register toward a first output; and  
 shifting photo charges in a second readout register toward a second output.

20. The method of claim 19, further including a step of repeating the first step and then the second step.

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21. The method of claim 19, further comprising steps of:  
combining photo charges at the first and second outputs; and  
converting the combined photo charges into a signal.
22. The method of claim 19, further comprising steps of:  
converting photo charges at the first output into a first signal;  
converting photo charges at the second output into a second signal; and  
combining the first and second signals into an output signal.
23. A method comprising steps of:  
collecting a first line of photo charges from a first line array of pixels;  
delaying the first line of charges;  
collecting a second line of charges from a second line array of pixels;  
shifting the delayed first line of charges toward a first output while  
simultaneously shifting the second line of charges toward a second output; and  
combining the first and second outputs.
24. The method of claim 23, wherein the first and second line arrays of pixels are  
co-parallel.

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